

Control of Multi phase Boost Type Switched Mode Rectifier

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Abstract— This project presents the Boost type switched Mode Rectifier (SMR), which is often used in many modern power circuitry to improve the output voltage regulation. Multiphase boost type SMR has advantage of high power density by incrementing number of stages. To keep the number of feedback signals fixed regardless of the topology and phase number N, with load current sensing is used. To improve the light-load efficiency, phase-shedding operation is implemented with load current sensing. (i.e., turning off some phases while switching to lesser load current).

Index Terms— phase-shedding operation, switched mode rectifier

I. INTRODUCTION

The qualified AC/DC conversion must meet the functions of input current shaping and output voltage regulation. The boost-type switch-mode rectifier (SMR), including a diode rectifier and a boost converter, is often used to perform the qualified Ac/Dc conversion. The conventional boost-type SMRs, the multiphase SMRs with an interleaved control scheme possess smaller current ripples and higher efficiency. Interleaving operation can be adopted to increase the power capacity, while still keep low current or voltage ripple. Due to the wide utilization of ac/dc power supply in electric systems, the problem of input harmonic current has been a big concern. This leads to the demand for electrical equipments to comply with the European Norm EN61000-3-2. Boost power factor correction (PFC) regulator has been used as a popular solution to suppress current harmonics, achieve unity power factor (PF), and utilize full line power [1]-[3]. To meet efficiency requirements, more and more multiphase boost-type SMRs were used in fuel-cell power-generation systems [4], Electric vehicle (EV) power conditioning systems usually

utilize a high-energy battery pack to store energy for the electric traction system [5], and photovoltaic applications [6]. Therefore, more and more research has focused on multiphase boost-type SMRs. Thus results [7]-[9] the light-load system efficiency can also be significantly improved by shutting down some boost cells (i.e., phase-shedding operation). Besides the phase-shedding technique, several other techniques are used to improve the light load efficiency of Dc–Dc converters such as pulse skipping, constant ON time techniques, mode hopping, or pulse frequency modulation. These techniques are suitable in lower load current applications such as a point of load (POL) converter or portable devices. However, these techniques do not fully take the thermal characteristics of semiconductor components into account to optimize the performance. It is designed by using a digital tool as a field-programmable gate array (FPGA); therefore, the operation for phase shedding is flexible, but the load switching point is not optimized because of the power loss is not involved in that method.

II. N-PHASE BOOST-TYPE

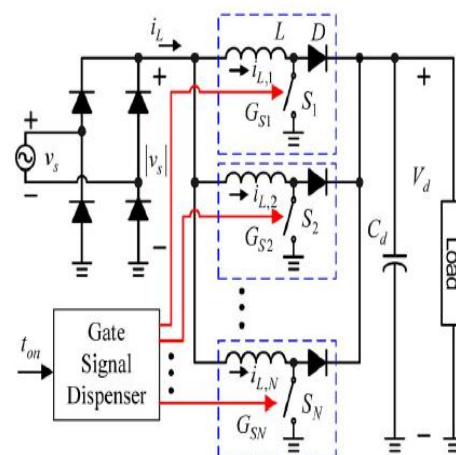


Fig. 1. Topology of an N-phase boost-type SMR

Fig. 1 shows the topology of an N-phase boost-type SMR, where integer N is the topology phase number (N>1). It consists of a diode bridge rectifier, N boost converters with the identical inductors and the identical diodes. To model the behavior of the N-phase boost-type SMR, some assumptions are initially made: 1) All switches are assumed to operate at a fixed period much smaller than the line period and thus, the input voltage over one switching period can be seen as a constant, and 2) a bulk capacitor is connected to the output dc voltage, and thus, the output voltage is assumed to be equal to its average value.

According to KCL, the total inductor current i_L is the sum of individual inductor currents

$$i_L = \sum_{k=1}^N i_{L,k} \quad (1)$$

When the input voltage $v_s(t) = V_{sp} \sin(2\pi t/T) = V_{sp} \sin(\omega t)$ is positive, the total inductor current i_L is equal to the input current i_s , and the current i_L is equal to the negative input current i_s when the input voltage v_s turns to negative. The input current can be represented in terms of the total inductor current i_L .

III. DESIGN OF INDUCTOR

To consider the practical condition, the nonzero inductor resistors are assumed. In addition, the effects of the voltage drops across the diode bridge rectifier, the freewheeling diode, and the semiconductor switch are also considered. The total voltage drop in the “switch-on” path is the sum of the voltage drops across the bridge rectifier and the semiconductor switch is also Zero.

$$L = \left(\frac{1}{f}\right) \times (V_{out} + V_F - V_{in_min}) \times \left(\frac{V_{in_min}}{V_{out} + V_F}\right) \times \left(\frac{1}{\Delta I_L}\right) \quad (2)$$

The frequency is 25KHZ if the value chosen below that current value will go to discontinuous mode within that half cycle.

V_{out} is the output voltage, V_f is the voltage drop across the diode $0.7 V_{MIN}$ = minimum Voltage of the Boost SMR, V_{MAX} = maximum Voltage of the Boost SMR

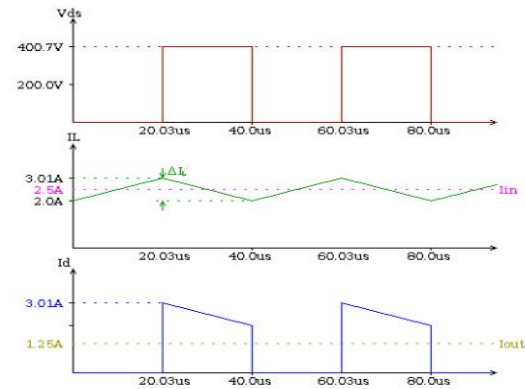


Fig. 2. Voltage and current waveform for boost SMR

Table I. Design of inductor for boost SMR

V_{in_min}	200V
V_{in_max}	380V
V_{in}	200V
$\Delta I_L V_{in_min}$	1A
I_{out}	1.25A
f	25KHZ
V_{out}	400V
L	4mH

Therefore, from (2), the behavior of the average total inductor current with the active-phase number n in an N-phase boost-type SMR can be equivalently modeled by a boost-type SMR, as shown in Fig. 2.

IV. DESIGN OF PROPORTIONAL CONTROLLER

The proposed method can be seen as a proportional-integral (PI)-type voltage controller illustrated in Fig. 3

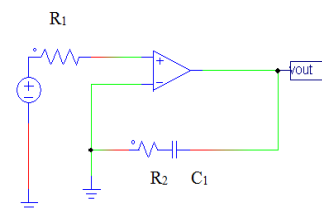


Fig.3. Circuit diagram of PI controller

$$\frac{U(S)}{E(S)} = \frac{R_1}{R_2} + \frac{1}{S C_1 R_1} \quad (3)$$

$$U(S) = \text{Output current}$$

$E(S)$ = Input current

R_1 = feedback resistor

R_2 = Input resistor.

C_1 = Filter capacitor

A. Design of the Differentiator

It is crucial to design a differentiator that can extract inductor voltage accurately. In addition, the differentiator should be capable of attenuating undesirable high-frequency component in and the injected noise, because derivative function is usually sensitive to high-frequency signals.

$$G_p = \frac{R_2}{R_1} = 1 \quad (4)$$

$$G_i = \frac{1}{R_2 C} = 2000 \quad (5)$$

Therefore from (4) G_p is proportional gain here both the resistors value is 10Ω . From (5) G_i is integral gain value is 10Ω and $0.5mF$. To avoid the effect of the double-line-frequency voltage ripple in the output voltage, the cutoff frequency is chosen to be smaller than the $1/20$ of the double line frequency is proposed in this design.

V. PHASE-SHEDDING OPERATION

At light load, more than one boost cell should be shut down to reduce the total switching loss and to increase the light-load efficiency. To work well under the phase-shedding operation, an adjustable gain (N/n) was included in this method. It is able to reduce the voltage dip due to the phase-shedding operation.

$$\theta = \frac{n}{N} \quad 1 \leq \text{integer } n \leq N \quad (6)$$

N = number of phases

n = number of active boost cells

θ = original phase shift angle

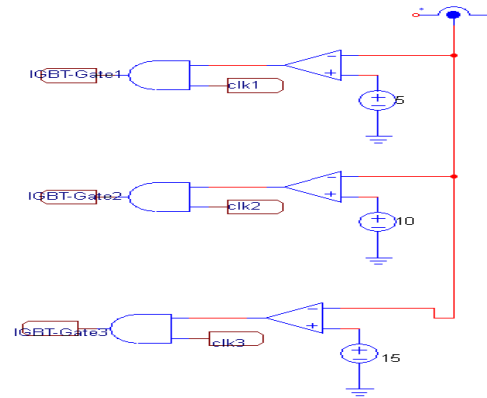


Fig.4. Circuit diagram of phase shedding operation

Table II Simulated Circuit Parameters

Input Voltage	230V
Switching frequency	25KHZ
Inductance	4mH
Capacitance	160uF
Resistance	300Ω

VI. SIMULATION RESULTS

In this section, a series of the computer simulations is provided to demonstrate the proposed boost-type SMR. The nominal values and the circuit elements are listed in Table II. The controller parameters were chosen as $G_p = 1 \text{rad/V}$ and $G_i = 2000 \text{rad/V/s}$. The simulation is done by using Psim software.

In fig.5. A single phase A.C. supply is given to the diode rectifier and current flows through the boost converter to the load output voltage is measured using voltage sensor. The input voltage is compare with zero detecting circuit and compared with the comparator. The output of the comparator compares the output from PI controller and given to ON-OFF controller. It provides the gate pulse for boost converter.

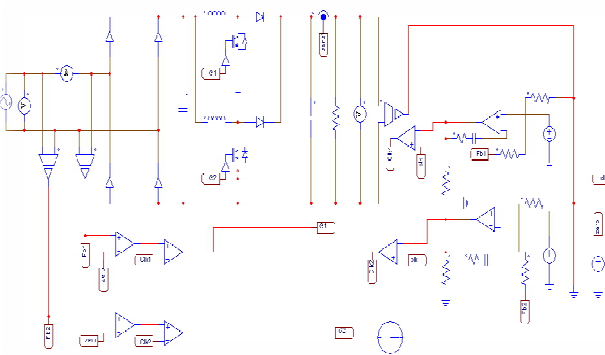


Fig.5 .Simulation Circuit for Single Phase Boost type SMR with Two Boost Cells

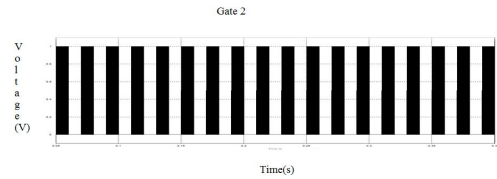


Fig .6(c) Pulse waveform for the Gate1 and Gate2

In Fig.6 (a) shows the output voltage single phase switched mode rectifier the average output voltage of the waveform is 390V. The above Fig.6 (b) shows the output current of single phase switched mode rectifier the average output current of the waveform is 1.3A.

In Fig 6(c) shows the pulse waveform for the Gate1 and Gate 2. Gate1 is ON for 0.02ms and Gate2 is ON for the next 0.04ms here the switching stress will be high because of continuous triggering pulses for both switches.

In Fig.7. A single phase A.C. supply is given to the diode rectifier and current flows through the boost converter to the load output voltage is measured using voltage sensor and output current measured using current sensor. The input voltage is compare with zero detecting circuit and compared with the comparator .The output of the comparator compares the output from PI controller and given to AND gate. The output of current sensor is given to the comparator output of AND gate is also compared with that comparator and if both inputs are high the switches will ON if it is low it will OFF. This is phase shedding operation

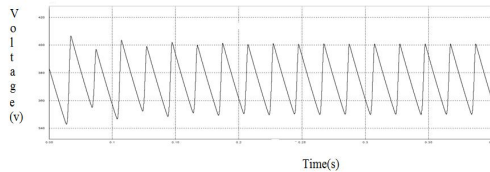


Fig.6 (a) Output Voltage of Single Phase SMR

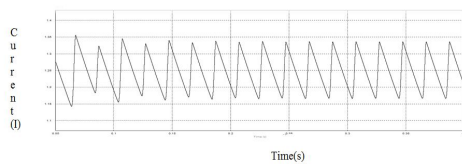


Fig.6 (b)Output Current of single phase SMR

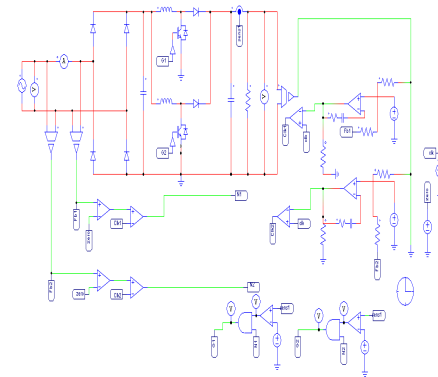
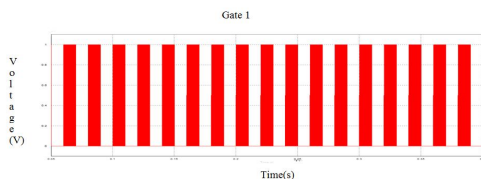


Fig.7. Single Phase Boost Type SMR with Phase Shedding with Two Boost Cells

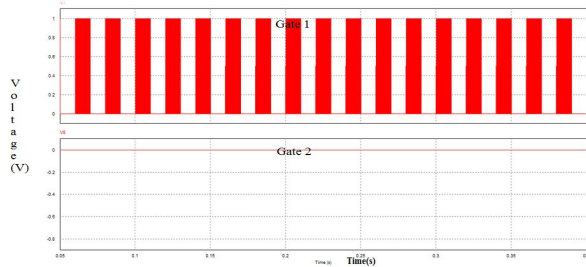


Fig.7(a) Pulse waveform for the Gate1 and Gate2

This condition will reset the flip-flop. This represents the RESET state of Flip-flop.

When $J=1, K=0$ In this case, the NAND gate corresponding to K becomes 0. Therefore Q becomes 0. This condition will set the Flip-flop. This represents the SET state of Flip-flop.

When $J=K=1$ In this case, $J=K=1$. This will cause the output to complement again and again. This complement operation continues until the Clock pulse goes back to 0.

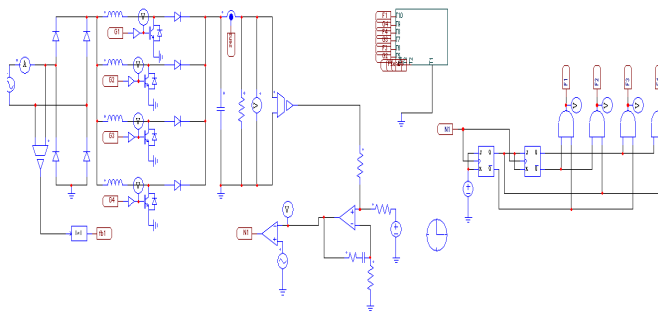


Fig.8 .Simulation Circuit for Single Phase Boost type SMR with Four Boost Cells

In Fig.7 (a) here the Gate 1 is on and Gate 2 is off so switching loss will be reduced overall efficiency will be increased.

In fig.8. A single phase A.C. supply is given to the diode rectifier and current flows through the boost converter to the load output voltage is measured using voltage sensor and output is given to PI controller and that output is given to the JK flip-flops and given to phase shedding operation to trigger gate pulse for boost converter.

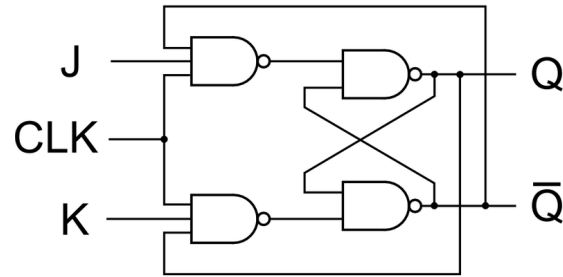


Fig.8 (a) Circuit diagram for a positive-edge-triggered JK flip-flop

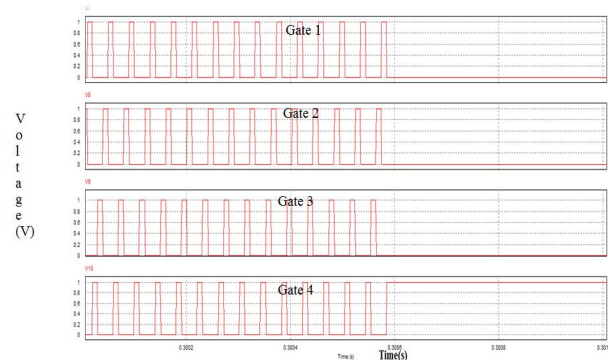


Fig.8 (b) Pulse waveform for two JK flip-flops

Table III Truth table for JK flip-flop

J	K	Q(t+1)	
0	0	Q(t)	No Change
0	1	0	Reset
1	0	1	Set
1	1	Q'(t)	Complement

When $J=0, K=0$ the output of the NAND gate corresponding to J becomes 0 .Therefore Q becomes 0.

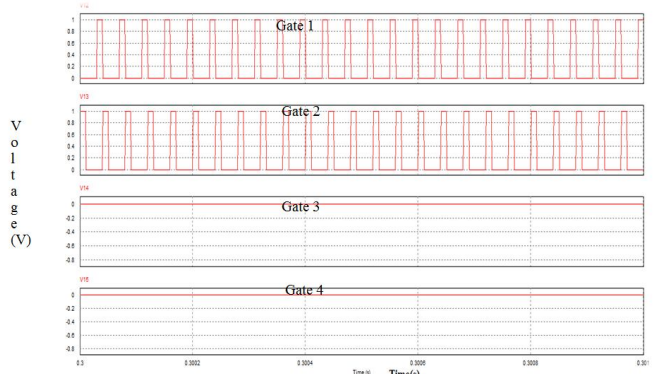


Fig.8(c) Pulse waveform for the Gate1, 2,3and 4

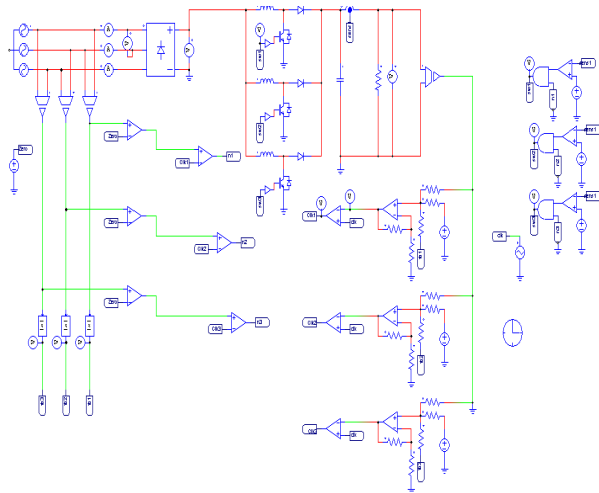


Fig.9. Three Phase Boost Type SMR with Phase Shedding with Three Boost Cells

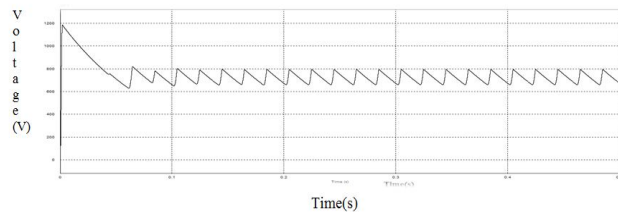


Fig.9 (a) Output Voltage of Three phase SMR

In Fig.8 (c) here the Gate 1,2 is on and Gate 3,4 is off so switching loss will be reduced overall efficiency will be increased. Power loss in that overall circuit is also reduced.

In Fig.9. A three phase A.C. supply is given to the diode rectifier and current flows through the boost converter to the load output voltage is measured using voltage sensor and output current measured using current sensor. The input voltage is compare with zero detecting circuit and compared with the comparator .The output of the comparator compares the output from PI controller and given to AND gate. The output of current sensor is given to the comparator output of AND gate is also compared with that comparator and if both inputs are high the switches will ON if it is low it will OFF. This is phase shedding operation.

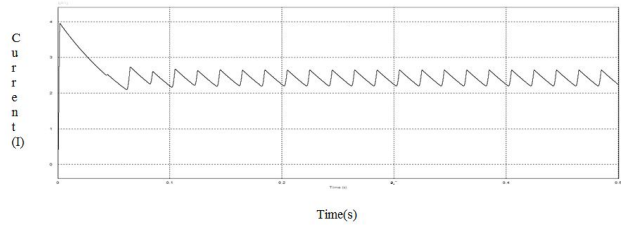


Fig.9 (b) Output Current of Three phase SMR

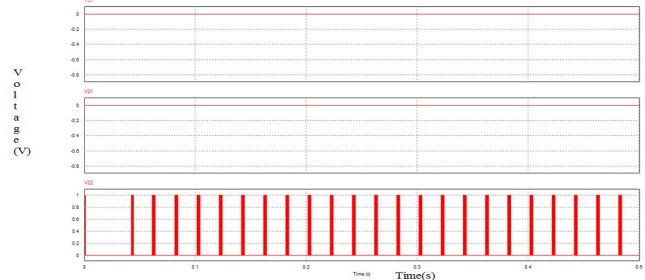


Fig 9(c) Pulse waveform for the Gate1, 2and Gate 3

Figure 9(a) shows the output voltage waveform of three phase switched mode rectifier the average output voltage of the waveform is 420V.

Fig.9 (b) output current waveform of three phase switched mode rectifier the average output current is 1.4A . In Fig.9 (c) here the Gate 3 is on and Gate1and 2 is off so switching loss will be reduced overall efficiency will be increased.

VII. CONCLUSION

The control of single phase and three phase SMR with phase shedding operation has been discussed and simulated. The proposed system has demonstrated very good performance with reduced switching losses and lesser number feedback signals and lesser number of sensors is used. Overall efficiency will be increased.

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ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

An ISO 3297: 2007 Certified Organization

Vol. 3, Special Issue 1, February 2014

National Conference on Innovation & Challenges in Electrical & Electronics Engineering (NCICEEE'14)

Organized by

Department of EEE, Sri Sairam Engineering College, West Tambaram, Chennai - 600 044, India on 18th February 2014

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